AMENDMENTS TO THE CLAIMS

1. (Original) An integrated circuit comprising:

a first die having:

a substrate with an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having:

a micro-electromechanical structure having an inductance;

a plurality of third bonding pads connected to the micro-electromechanical structure; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

2. (Currently amended) The integrated circuit of claim 1 and further comprising:

a ~~semiconductor~~ package, the ~~semiconductor~~ package having a plurality of fourth bonding pads, a plurality of circuit board connectors, and internal routing that electrically connects the plurality of fourth bonding pads to the plurality of circuit board connectors, the first die being attached to the ~~semiconductor~~ package; and

a plurality of wires connected to the first bonding pads and the fourth bonding pads.

3. (Currently Amended) The integrated circuit of claim 1 wherein the second die further includes a capacitive micro-electromechanical structure that has a capacitance.

Claims 4-20. (Cancelled.)

21. (New) The integrated circuit of claim 1 wherein the plurality of connectors includes solder.

22. (New) The integrated circuit of claim 1 wherein

the passivation layer has a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region;

the plurality of first bonding pads are formed on the passivation layer only in the peripheral region; and

the plurality of second bonding pads are formed on the passivation layer only in the center region.

23. (New) The integrated circuit of claim 1 wherein a portion of a third bonding pad is substantially vertically aligned with a portion of a second bonding pad.

24. (New) The integrated circuit of claim 2 wherein the package has a top surface and a bottom surface, the plurality of fourth bonding pads are located on the top surface, and the plurality of circuit board connectors are located on the bottom surface.

25. (New) An integrated circuit comprising:

a first die including:

a substrate having an electrical circuit;

an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect, the passivation layer having a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region;

a plurality of first bonding pads formed on the passivation layer only in the peripheral region, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer only in the center region, the second bonding pads being electrically connected to the interconnect;

a second die having a plurality of third bonding pads; and

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads.

26. (New) The integrated circuit of claim 25 wherein a portion of a third bonding pad is substantially vertically aligned with a portion of a second bonding pad.

27. (New) The integrated circuit of claim 25 wherein the plurality of connectors includes solder.

28. (New) The integrated circuit of claim 25 wherein the second die includes a micro- electromechanical structure.

29. (New) The integrated circuit of claim 28 wherein the micro-electromechanical structure has inductance.

30. (New) The integrated circuit of claim 28 wherein the micro-electromechanical structure has capacitance.

31. (New) The integrated circuit of claim 28 wherein the first die does not include a micro-electromechanical structure.

32. (New) An integrated circuit device comprising:

a first die including:

a substrate having an electrical circuit;

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an interconnect formed on the substrate and electrically connected to the electrical circuit;

a passivation layer formed on the interconnect;

a plurality of first bonding pads formed on the passivation layer, the first bonding pads being electrically connected to the interconnect;

a plurality of second bonding pads formed on the passivation layer, the second bonding pads being electrically connected to the interconnect;

a second die having a plurality of third bonding pads;

a plurality of connectors electrically connected to the second bonding pads and the third bonding pads;

a package including:

a substrate having a top surface and a bottom surface, the substrate being attached to the first die;

a plurality of fourth bonding pads formed on the top surface of the substrate;

internal routing electrically connected to the fourth bonding pads;

a plurality of circuit board connectors formed on the bottom surface of the substrate, the circuit board connectors being connected to the internal routing; and

a plurality of bonding wires, the wires connecting the first bonding pads to the fourth bonding pads.

33. (New) The integrated circuit device of claim 32 wherein the plurality of circuit board connectors include solder regions.

34. (New) The integrated circuit device of claim 33 wherein the plurality of circuit board connectors include pins.

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35. (New) The integrated circuit of claim 33 wherein the plurality of connectors includes solder.

36. (New) The integrated circuit of claim 33 wherein

the passivation layer has a top surface, a center region of the top surface, and a peripheral region of the top surface that surrounds the center region;

the plurality of first bonding pads are formed on the passivation layer only in the peripheral region; and

the plurality of second bonding pads are formed on the passivation layer only in the center region.

37. (New) The integrated circuit of claim 33 wherein a portion of a third bonding pad is substantially vertically aligned with a portion of a second bonding pad.